REMARKS

Claims 1, 5, 8, 11, 12, 14, 19-21 and 23 have been amended. Claims 4, 10, 13, 17 and 18 have been canceled. Claims 1-3, 5-9, 11, 12, 14-16 and 19-23 remain in the application. Applicant respectfully requests further examination of the application, as amended.

Rejection of Claims 4-7, 10-13 and 17 Under 35 U.S.C. § 112, ¶ 2

Claims 4-7, 10-13 and 17 stand rejected under 35 U.S.C. § 112, second paragraph, on the grounds that they are unclear because they allegedly recite or imply that bit error correction is performed when no errors are detected. Independent claims 1, 8, 14, 21 and 23 have been amended in a manner that is believed to clarify this aspect of the invention. More specifically, independent claims 1, 8 and 14 have been amended to incorporate and clarify the subject matter of dependent claims 4, 10 and 17, now canceled. (Independent claim 23 has also been amended in a similar manner, as discussed below.) Applicant believes that that all claims, as amended, now particularly point out and distinctly claim the subject matter to which they are directed.

A problem with prior bit error detectors that the invention addresses is that prior detectors can inherently multiply bit error indications. That is, for each erroneous bit, the prior detector can output not just one error indication but rather some number *n* of such error indications (where *n* is a factor that depends upon the configuration of the detector shift register). This phenomenon is described in Applicant's specification at page 4, line 7 through page 5, line 7. More specifically, such a prior bit error detector will output multiple (*n*) error indications in an instance in which only one erroneous bit occurs within a certain interval (which depends upon the shift register configuration and can be readily determined). However, in an instance in which two or more such erroneous bits occur within such an interval of each other, the detector will output a number of error indications that is less than n.

The claimed invention addresses the above-described problem by correcting each erroneous bit that does not occur within the above-mentioned interval of another erroneous bit. Stated another way, it corrects only isolated erroneous bits and does not attempt to correct bursts of erroneous bits. In summary, as stated on page 18, lines 5-7 of Applicant's specification, correction of an erroneous bit is suppressed or disabled if another erroneous bit is detected during the interval. The interval can be defined by a number of clock cycles, i.e., bit periods, or by a time interval.

As amended, independent claims 1 and 23 recite that the trigger circuit responds to an erroneous bit by disabling the correction circuit until it is determined that the predictor circuit no longer contains erroneous bits. The amended claim clarifies what is claimed and confirms the Examiner's observation on page 3 of the Office Action that an error indeed must first be detected before the trigger circuit operates.

As amended, independent claim 8 recites that the trigger circuit responds to an erroneous bit by disabling the third logic element from correcting any bits until it is determined that the shift register no longer contains erroneous bits. The amended claim similarly clarifies what is claimed and confirms the Examiner's observation on page 3 of the Office Action that an error indeed must first be detected before the trigger circuit operates.

As amended, independent claim 14 recites that, in response to the error signal, correcting the erroneous bit is disabled until it is determined that no additional error signal has been provided during a predefined interval. The amended claim likewise clarifies what is claimed and confirms the Examiner's observation on page 3 of the Office Action that an error indeed must first be detected before the trigger circuit operates.

As amended, independent claim 21 recites that a means for disabling the corrector responds to an error signal by disabling the predictor from correcting the erroneous bit until it is determined that the predictor no longer contains erroneous bits. The amended claim thus clarifies what is claimed and confirms the Examiner's observation on page 3 of the Office Action that an error indeed must first be detected before the trigger circuit operates.

Rejection of Claims 1-3, 8, 9, 14-16 and 18-22 Under 35 U.S.C. § 102(e)

Claims 1-3, 8, 9, 14-16 and 18-22 stand rejected under 35 U.S.C. 102(e) as being anticipated by *Reberga* (U.S. Patent Application Publication No. 2004/0128603). As Applicant has amended independent claims 1, 8, 14 and 23 to incorporate the subject matter of claims (now canceled) that were not subject to a rejection based on patentability over the prior art but rather only subject to the above-discussed Section 112 rejection, Applicant respectfully submits that amended claims 1, 8, 14 and the claims that depend therefrom are likewise patentable over *Reberga*.

Rejection of Claim 23 Under 35 U.S.C. § 102(e)

Claim 23 stands rejected under 35 U.S.C. 102(e) as being unpatentable over *Reberga* in view of *Rakib* (U.S. Patent Application Publication No. 2001/0001616). Claim 23 recites

limitations similar to those recited in claim 1 but further includes additional elements of a high-speed communication system. *Rakib* is cited only for teaching a communication system. As Applicant has amended independent claim 23 to incorporate the subject matter of claims (now canceled) that were not subject to a rejection based on patentability over the prior art but rather only subject to the above-discussed Section 112 rejection, Applicant respectfully submits that claim 23, as amended, is likewise patentable over *Reberga* and *Rakib.*

CONCLUSION

In view of the foregoing, Applicant respectfully submits that all grounds of rejection have been successfully traversed and/or overcome and that that application is now in condition for allowance. Should the Examiner have any comment regarding Applicant's response or believe that a teleconference would expedite examination of the pending claims, Applicant requests that the Examiner telephone Applicants' undersigned attorney.

Respectfully submitted,

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